
2009 International Conference on Semiconductor Technology for Ultra Large Scale Integrated Circuits and Thin Film Transistors (ULSIC vs. TFT)

Editor:

Y. Kuo

Texas A&M University
College Station, Texas, USA

Sponsoring Division:



Electronics and Photonics



Published by
The Electrochemical Society

65 South Main Street, Building D
Pennington, NJ 08534-2839, USA

tel 609 737 1902

fax 609 737 2743

www.electrochem.org

ecstransactions™

Vol. 22 No. 1

Copyright 2009 by The Electrochemical Society.
All rights reserved.

This book has been registered with Copyright Clearance Center.
For further information, please contact the Copyright Clearance Center,
Salem, Massachusetts.

Published by:

The Electrochemical Society
65 South Main Street
Pennington, New Jersey 08534-2839, USA

Telephone 609.737.1902
Fax 609.737.2743
e-mail: ecs@electrochem.org
Web: www.electrochem.org

ISSN 1938-6737 (online)
ISSN 1938-5862 (print)

ISBN 978-1-56677-736-4 (CD-ROM)
ISBN 978-1-60768-085-7 (PDF)

Printed in the United States of America.

PREFACE

This issue of *ECS Transactions* includes 33 papers that were presented at the Second International Conference on Semiconductor Technology for Ultra Large Integrated Circuits and Thin Film Transistors (ULSIC vs. TFT II), held in the Xi'an Garden Hotel, Xian, China, July 5-10, 2009. This symposium was sponsored by the Engineering Conferences International.

This conference provided a forum on the latest developments in the two largest semiconductor industries, i.e., ULSIC and TFT-LCD. Global experts from universities, industry, and governments exchanged their experience, knowledge, and visions through technical presentations and discussions during the presentation time, brainstorming sections, and afternoon and evening breaks. Future scientific and technology challenges were forecasted and debated. A large number of graduate students from various countries presented poster papers and were engaged in discussions. Participants were from Belgium, Canada, China, France, Germany, Hong Kong, India, Japan, Korea, Singapore, Netherlands, Taiwan, UK, and the USA.

The plenary speeches were dedicated to 1) Technology Development Strategy of Chinese IC Fabrication by T. Ye of Institute of Microelectronics, Chinese Academy of Sciences, Beijing, 2) An Overview of NEDO's Electronics Technology Development Projects by A. Ando of NEDO, Japan, and 3) Reliability and Optimization by W. Kuo of City University of Hong Kong. In total, 81 papers were scheduled into the following sections:

- Plenary
- Modeling, Simulation, and Scaling
- Challenges in ULSI Gate Dielectrics–
- Challenges in Si-based TFT Technology
- Challenges in ULSI Substrates and Materials
- Challenges in TFT Materials-
- Challenges in Advanced ULSI Processes-
- Challenges in Flexible Electronics
- Challenges in New Devices and Applications-
- Challenges in Nano Devices
- Posters

The conference also included three panel sessions on 1) Challenges in Devices and Scaling, 2) Challenges in Materials and Applications, and 3) Challenges in ULSIC and TFT Fabrications.

In order to present subjects in a coherent manner, papers in this issue of *ECS Transactions* have been arranged into six sections. All manuscripts are published as originally received, without alteration of technical contents.

The success of this conference is contributed by seamless efforts among conference co-chairs Professors M. Shur, W. Milne, S. Xiong, and D. Ast, who were

involved in coordination, organization, and collaboration of many critical activities. The local chair Professor C. Liu and committee member Professor S. Wu played important roles in communicating with central and local Chinese governments and the Xi'an Jiaotong University as well as offering many valuable advices and services.

The following people are greatly appreciated for various conference activities:

- Plenary and invited speakers for their presentations and panel discussions
- Session chairs for conducting the meeting
- Authors and presenters for their participation
- Scientific advisory committee members for their contributions in planning and coordinating the program
- Dr. N. Li for valuable suggestions and serving as the conference ECI liaison
- Mr. C.-H. Lin for his administrative supports
- ECI staffs for effectively management of the conference
- the Staff of the Electrochemical Society for professional work in publishing this issue of ECS *Transactions*.

Yue Kuo
Texas A&M University

Acknowledgements

Conference chairs express their sincere thanks to the generous sponsorship of:

Semiconductor Energy Laboratory
Electrochemical Society Electronics and Photonics Division

Conference chairs also thank the valuable technical sponsorship from:

Electrochemical Society Electronics and Photonics Division
Japan Society of Applied Physics
Korean Physical Society Semiconductor Division
MRS-Taiwan
Sematech
IMEC
National Natural Science Foundation of China
Xi'an Jiaotong University

Conference Co-chairs

Yue Kuo, Texas A&M University
Michael Shur, Rensselaer Polytechnic Institute
Dieter Ast, Cornell University
William Milne, Cambridge University
Shaozhen Xiong, Nankai University

Local Committee Chair

Chunliang Liu, Xi'an Jiaotong University

Local Organizing Committee

Shengli Wu, Xi'an Jiaotong University
Jinhai Si, Xi'an Jiaotong University
Zhihu Liang, Xi'an Jiaotong University

Scientific Advisory Committee

G. Bersuker, Sematech	S. Higashi, Hiroshima U.
O. Bonnaud, U. de Rennes I	H. P. Hsieh, National Chiao Tung U.
I. Boyd, U. College London	R. Huang, Peking U.
D. N. Buckley, U. Limerick	J. Jang, Kyung Hee U.
G. Celler, Soitec	T. P. Ma, Yale U.
T. C. Chen, IBM Watson Research Center	J. Murota, Tohoku U.
C. Claeys, IMEC	J. Peterson, Albany Nano Tech
S. Fonash, Pennsylvania State U.	A. Nathan, U. College London
S. Hamaguchi, Osaka U.	R. Street, PARC
M. K. Han, Seoul National U.	S. Uchikoga, Toshiba
M. Hatano, Hitachi	Y. Yamamoto, Sharp

Session Chairs

G. Bersuker, Sematech	J. Murota, Tohoku U.
O. Bonnaud, U. Rennes 1	A. Nathan, U. College London
C. Claeys, IMEC	B.-Y. Nguyen, Soitec
S. Fonash, Pennsylvania State U.	K. L. Pey, Nanyang Technological U.
M. Hatano, Hitachi	D. Privat, Ecole Polytechnique, Palaiseau
R. Huang, Peking U.	J. Stathis, IBM
R. Ishihara, Delft U. of Technology	M. Shur, RPI
J. Jang, Kyung Hee U.	F. Templier, CEA-LETI Minatec
Y. Kuo, Texas A&M U.	S. Xiong, Nankai U.
T. P. Ma, Yale U.	O. Weber, CEA-LETI
W. Milne, Cambridge U.	C. Wu, Nankai U.

Table of Contents

Preface *iii*

Chapter 1 Challenges in ULSI Gate Dielectrics

Nanoscale Gate Stacks: From Atomic Defects to Device Performance *	3
<i>G. Bersuker, C. Park, J. Price, P. Lysaght, P. Kirsch and R. Jammy</i>	
Impact of Gate Dielectric Breakdown Induced Microstructural Defects on Transistor Reliability *	11
<i>X. Li, K. Pey, V. Lo, R. Ranjan, C. Tung and L. Tang</i>	
Time-to-Breakdown Behavior and Mechanism on U-grooved n-MOSFET	27
<i>J. Seo, H. Park, G. Kang, J. Kang and B. So</i>	

Chapter 2 Challenges in Si-based TFT Technology

TFT Technology Programs in China *	35
<i>S. Xiong, Z. Meng, C. Wu, J. Li, J. He and F. Zhang</i>	
From Amorphous-Si Thin-Film-Transistors to Single Crystal-Si Transistors: Influence of Si Crystallinity on Device Properties *	49
<i>F. Templier</i>	
Single Grain Si TFTs for RF and 3D ICs *	57
<i>R. Ishihara, A. Baiano, T. Chen, J. Derakhshandeh, M. D. Tajari Mofrad, M. Danesh, N. Saputra, J. R. Long and C. I. Beenakker</i>	

Chapter 3

Challenges in ULSI Substrates, Materials and Processes

High Scalability and Low Variability of Planar Fully Depleted SOI MOSFETs *	71
<i>O. Weber, F. Andrieu, C. Fenouillet-Béranger, C. Buj-Dufournet, V. Barral, P. Perreau, L. Tosti, L. Brevard and O. Faynot</i>	
Selective Epitaxy of Si and SiGe for Future MOS Devices *	81
<i>I. Mizushima</i>	
Substrate Engineering for 32nm and Beyond *	91
<i>B. Nguyen, C. Mazuré and G. Celler</i>	
Defect Aspects of Ge-on-Si Materials and Devices *	99
<i>C. Claeys, G. Eneman, G. Wang, L. Souriau, R. Loo and E. Simoen</i>	
Atomically Controlled Processing for Group IV Semiconductors *	111
<i>J. Murota and M. Sakuraba</i>	
Atomic Layer Doping for Future Si Based Devices *	121
<i>B. Tillack and Y. Yamamoto</i>	
16kb Phase Change Memory Test Chip with 0.18- μ m Process	133
<i>S. Ding, Z. Song, B. Liu, D. Cai, X. Chen, Y. Chen, M. Zhong, G. Feng, C. Xu, S. Feng, Z. Xie, Z. Yang, X. Wan, F. Zhang, G. Wu and Y. Xiang</i>	
Dry Etching of Nanosized Si ₂ Sb ₂ Te ₅ Patterns using TiN Hard Mask for High Density Phase-change Memory	145
<i>G. Feng, Z. Song, B. Liu, S. Feng and B. Chen</i>	
Ultra Thin Oxide by Chemical Vapour Oxidation of Si	151
<i>B. J. Kailath, A. DasGupta and N. DasGupta</i>	
Effect of Ge ₂ Sb ₂ Te ₅ Material Properties on its CMP Process	161
<i>M. Zhong, Z. Song, B. Liu, S. Feng, F. Zhang and Y. Xiang</i>	
Atomic Vapor Deposition of TiN with Diluted Tetrakis (diethylamido) Titanium (TDEAT) for Phase Change Memory	167
<i>L. Wang, B. Liu, Z. Song, S. Feng, Z. Zhou, Y. Xiang and F. Zhang</i>	
Surface Roughening and Microstructure of Tantalum Nitride Films Sputtered at Different N ₂ /Ar Flow Ratios	175
<i>J. J. Yang, B. Liu, Y. Wang and K. W. Xu</i>	

Chapter 4

Challenges in Advanced TFT Processes

A-Si:H TFT Nonvolatile Memories and Copper Interconnect for Rigid and Flexible Electronics *	183
<i>Y. Kuo</i>	
Metal induced crystallized poly-Si Thin Films and Thin Film Transistors	191
<i>C. Wu, Z. Meng, S. Zhao, X. Li, Z. Liu, J. Li, M. Wang, H. Kwok and S. Xiong</i>	
Stability Study of ZnO TFT using a Simple and Effective Model	201
<i>C. Dong, J. Li, B. Jin, D. Bub and Y. Su</i>	
Design of poly-Si TFT Shift Register and Latch Circuit by PMOS Process	207
<i>P. Sun, C. Wu, Z. Meng, Y. Yao, L. Zhao and S. Xiong</i>	

Chapter 5

Challenges in Modeling, Simulation, and Scaling

Model and Key Fabrication Technologies for FeRAM *	217
<i>T. Ren, M. Zhang, Z. Jia, L. Wang, C. Wei, K. Xue, Y. Zhang, H. Hu, D. Xie and L. Liu</i>	
Down-scaling of Thin-Film Transistors: Opportunities and Design Challenges	227
<i>X. Guo, R. Sporea, J. Shannon and S. R. Silva</i>	
Simulation of SET process in Phase-Change Random Access Memory by Three-Dimension Finite Element Modeling	239
<i>Y. Gong, Z. Song, Y. Ling, B. Liu, Y. Liu and S. Feng</i>	
Three-dimensional Finite Element Analysis of Phase Change Memory Cell with Thin TiO ₂ Stop Layer used for Forming Deep Sub-micro Electrode	249
<i>Y. Liu, Z. Song, Y. Ling and S. Feng</i>	

Chapter 6

Challenges in New and Nano Devices and Applications

Bipolar Device and Circuit Technologies for Future Wireless Communications *	261
<i>K. Washio, N. Shiramizu, M. Miura, T. Nakamura, K. Oda and T. Masuda</i>	

Novel Asymmetric Tunneling Devices for Low Power ULSI *	273
<i>N. Venkatagirish, A. Tura, R. Jhaveri, H. Chang and J. C. Woo</i>	
SOI CMOS Platform for Gas Sensing Applications *	281
<i>W. I. Milne, S. Santra, F. Udrea, S. Ali, P. Guha, S. Vieira, S. Maeng and J. Gardner</i>	
Vertical Channel Thin Film Transistor Technology: Similar Approach with 3D-ULSI Monolithic Technology *	293
<i>O. Bonnaud</i>	
Lateral Porous Alumina Templates for Planar Organisation of Carbon Nanotubes and Semiconductor Nanowires *	305
<i>D. Pribat, M. Gowtham, C. Cojocar and B. S. Kim</i>	
Fabrication and Transport Behavior Investigation of Gate-All-Around Silicon Nanowire Transistor from Top-Down Approach *	317
<i>R. Huang, R. Wang, Y. Tian, J. Zhuge, L. Zhang, C. Liu, Y. Wang, Y. Ai and Y. Wang</i>	
Breakdown of Small Diameter Si Nanowires under External Electric Field: First-principle Calculation	327
<i>R. Zhang, N. Gao, Z. Wen and Q. Jiang</i>	
Author Index	335

* = *invited paper*